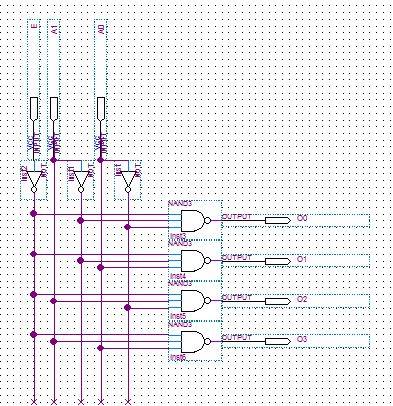
**Objectives:**

1. To implement and test a 2-to-4 lines decoder and with active-LOW outputs and active-LOW enable input using random gates.

2. To implement and test combinational logic functions using IC 74138 (3-to-8-lines decoder with active-LOW outputs).

**Answer to the Pre-Lab Questions:**

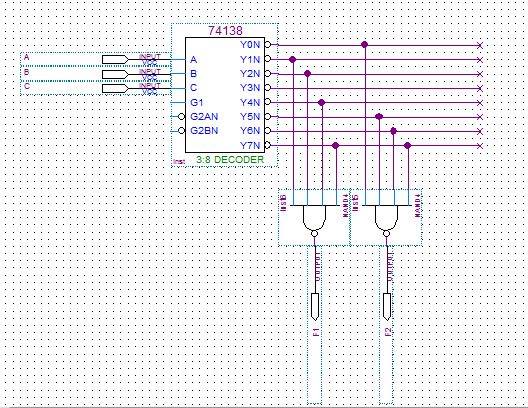
**1.**



2.

|  |  |
| --- | --- |
| E A1 A0 | O3 O2 O1 Oo |
| 0 0 0 | 1 1 1 0 |
| 0 0 1 | 1 1 0 1 |
| 0 1 0 | 1 0 1 1 |
| 0 1 1 | 0 1 1 1 |
| 1 0 0 | 1 1 1 1 |
| 1 0 1 | 1 1 1 1 |
| 1 1 0 | 1 1 1 1 |
| 1 1 1 | 1 1 1 1 |

3.



**EAST WEST UNIVERSITY**

**Semester:** Fall 2016

**Course Number:** CSE 345

**Course Title:** Digital Logic Design

**Experiment No:** 05

**Experiment Title:** Decoder and its use in combinational logic implementation

**Name:** Md. Sakibur Rahman

**ID:** 2014-1-60-032

**Group Number:** 02

**Group IDs:**

2014-1-60-032

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2014-1-60-030

2014-1-60-055

**Date of Performance:** November 16, 2016